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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/523,132	03/10/2000	Yasunao Okazaki	10873.506US01	6038

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EXAMINER

LEE, BENNY T

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES DEPARTMENT OF COMMERCE  
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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/523,132			

EXAMINER	
ART UNIT	PAPER NUMBER
14	

DATE MAILED:

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined  Responsive to communication filed on 12 May 2002  This action is made final.

A shortened statutory period for response to this action is set to expire Three (3) month(s), 0 days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1.  Notice of References Cited by Examiner, PTO-892. 2.  Notice re Patent Drawing, PTO-948.  
3.  Notice of Art Cited by Applicant, PTO-1449 4.  Notice of Informal Patent Application, Form PTO-152  
5.  Information on How to Effect Drawing Changes, PTO-1474 6.

Part II SUMMARY OF ACTION

2-17

1.  Claims \_\_\_\_\_ are pending in the application.

Of the above, claims \_\_\_\_\_ are withdrawn from consideration.

2.  Claims \_\_\_\_\_ have been cancelled.

3.  Claims \_\_\_\_\_ are allowed.

4.  Claims 2-4, 6-10; 11-13, 15-17 are rejected.

5.  Claims 5; 14 are objected to.

6.  Claims \_\_\_\_\_ are subject to restriction or election requirement.

7.  This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.

8.  Allowable subject matter having been indicated, formal drawings are required in response to this Office action.

9.  The corrected or substitute drawings have been received on \_\_\_\_\_. These drawings are  acceptable;  
 not acceptable (see explanation).

10.  The  proposed drawing correction and/or the  proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_,  
has (have) been  approved by the examiner.  disapproved by the examiner (see explanation).

11.  The proposed drawing correction, filed \_\_\_\_\_, has been  approved.  disapproved (see explanation). However,  
the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are  
corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO  
EFFECT DRAWING CHANGES", PTO-1474.

12.  Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has  been received  not been received

been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.

13.  Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in  
accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14.  Other

EXAMINER'S ACTION

SN 523132

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### **DETAILED ACTION**

The following claims have been found objectionable for reasons set forth below:

In claims 2, 11, next to last line in each claim, note that “another input/output line” should be rephrased as --another of said input/output lines-- for consistency of description.

In claim 11, line 2, note that “formed” should be rewritten as --disposed--.

In claims 12, 14, note that “made” should be rewritten as --comprised--.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2-4, 8, 9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Deki et al.

Deki et al discloses in fig. 1 thereof, a high frequency circuit comprising a dielectric substrate (4) having high frequency input/output lines (1, 3) disposed thereon. The substrate is disposed in a metal casing or box (8) such that a shielding effect is provided for the substrate by the box. Note that input/output terminals (9, 10) respectively connect to high frequency input/output lines (1, 2). A conductive partition plate (7) is disposed in and attached to the box such a to divide the internal space of the box, thereby to separate a region with input/output line (1) from a region with input/output line (3). Accordingly, the partition plate (7) suppresses the

generation of undesired modes of wave propagation by cutting off the path of propagation of such waves.

With respect to claims 8, 9, note from fig. 3 of Deki et al that the high frequency circuit comprises a high frequency filter (18) having a coupled resonator configuration.

Claims 2-4, 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Deki et al.

Nishimura (Fig. 2) discloses high frequency circuit comprising a substrate having input/output lines (1) disposed thereon and associated with semiconductor device (2). The substrate, input/output lines and the semiconductor device are disposed in a metal casing or box (3) to provide a shielding effect. A cover (5) is disposed to close off the case (3). The cover contains a conductive plate shape partition protruding from an inner surface thereof. The conductive partition plate is positioned such as to separate the respective input/output lines (1) into separate regions. Accordingly, the partition plate functions to suppress undesired waveguide modes from propagating between the input/output line regions. Also, with respect to claim 6, note that as evident from fig. 2 the partition plate is oriented perpendicular to the direction of propagation. Moreover, with respect to claim 7, as evident from Fig. 1(b), the partition plate provides a space or cut-out region relative to the casing. However, Nishimura differs from the claimed invention in that the input/output lines are not operatively connected to input/output terminals which are located on the casing or box, as recited in the claimed invention.

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As described above, Deki et al discloses a high frequency circuit disposed in a case and having input/output lines thereof connected with input/output terminals located on the casing or box.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have modified the casing or box of Nishimura to have included input/output terminals. Such a modification would have been considered obvious since it would have provided the advantageous benefit of providing external connections to the high frequency circuit, thereby suggesting the obviousness of such a modification.

Claims 11-13, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deki et al in view of Tsuji (of record).

As described above, Deki et al discloses the claimed invention except for the location of "covers" over the respective input/output lines/terminals, as recited in these claims.

Tsuji discloses a high frequency circuit element having a metal box (1, 2) containing a high frequency circuit (3a, 3b) therein disposed on a substrate (4). As is evident from fig. 4, input/output terminals (6a, 6b) are disposed in the metal box and are connected to input/output lines (5a, 5b) which are associated with the high frequency circuit (3a, 3b). A cover member (8, 9) is disposed over the high frequency circuit (3a, 3b) as well as the input/output lines (5a, 5b) such as to increase the cutoff frequency. Furthermore, note that because of the nature of the "cover", such a structure would also have been characterized as being a "plate". Note that an increase in cutoff frequency inherently results in cutting off, and thus suppressing, those electromagnetic

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modes which are outside the range of the cutoff frequency. Furthermore, note that the cover members (8, 9) longitudinally divide the metal box supporting the high frequency circuit by one-half, thereby providing the increased cutoff frequency and corresponding mode suppression.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have added the longitudinal "covers" to the longitudinally partitioned metal box of Deki et al. Such a modification would have been considered obvious in view of the same field of endeavor of the references (i.e. both pertain to metal boxes with high frequency circuits therein with means for suppressing unwanted modes), thereby suggesting the obviousness of such a modification. Moreover, note that since the partition (7) of Deki et al and the "cover" (8, 9) of Tsuji are oriented along the same longitudinal orientation, the addition of such "covers" would have been compatible with the partition orientation in Deki et al, thereby further suggesting the obviousness of such a modification.

With respect to claims 15, 16, note from fig. 3 of Deki et al that the high frequency circuit comprises a high frequency filter (18) having a coupled resonator configuration.

Claims 10; 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the preceding rejection as applied to claims 2 & 11, respectively above in view of Buck et al (of record) for reasons of record.

Applicant's arguments with respect to claims 2-4, 6-10; 11-13, 15-17 have been considered but are moot in view of the new ground(s) of rejection.

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Claims 5, 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

It is suggested by the examiner that, prior to the filing of applicants' next response, perhaps an interview be undertaken between the applicants' and the examiner as a means of understanding the inventive concept & the proper scope of potential claim coverage and thus possibly expediting prosecution.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benny Lee whose telephone number is (703) 308 4902.



BENNY T. LEE  
PRIMARY EXAMINER  
ART UNIT 2817

B. Lee

July 18, 2003